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LEAKAGE CURRENT CONTROL BY CIRCUIT TECHNIQUES

DVTS

Dynamic Voltage & Threshold SCALING

DVTS IS IMPROVED VERSION OF DVS AS IT CAN BE ACHIEVED AT MOST TECHNOLOGY NODES (SCALING)

DVS

We have a Single Loop here.

V_{DD} IS ADJUSTED FOR SPEED PERFORMANCE

VOLTAGE – FREQUENCY RELATION STORED IN LOOK-UP Table

"MOST COMMONLY USED TECHNIQUE"

NPTEL

(b). DVC gets this Information And Which then Allows V_{DD} to REGULATE.

. CONDITION THAT THIS MEETS CRITICAL PATH DELAY

(C) DELAY IS FED BACK TO DFC

TWO LOOPS ACHIEVE STABLE VALUES FOR V_{DD} AND f

TWO CLOSED-LOOPS in DVFS

1. Dynamic Voltage Control → DVC
2. Dynamic Frequency Control → DFC

Steps in Control:

a. DFC MONITORS CHIP-ACTIVITY
$\Rightarrow$ DECIDES FREQUENCY TO WORK AT

NPTEL

'Dynamic Voltage and Frequency Scaling'

DVFS

We have $P_{Dynamic} \propto V_{DD}^2$

$\propto f$

Reducing V_{DD} => $P_{DYNAMIC}$ REDUCES

=> REDUCES $P_{LEAKAGE}$

AS $V_{DD}\downarrow$ reduces V_{TH} through Change in DIBL

ADAPTIVE BIASING

VARIABLE V_{TH} CMOS

(VTCMOS)

[A] ACTIVE MODE → BACK-BIAS SET TO '0'

TRANSISTORS HAVE LOW V_{TH}.

[B] 'OFF STAND-BY' → BACK-BIAS SET TO HIGH REVERSE BIAS

TRANSISTORS ARE NOW HAVING HIGHER V_{TH} ⇒ LOWER LEAKAGE

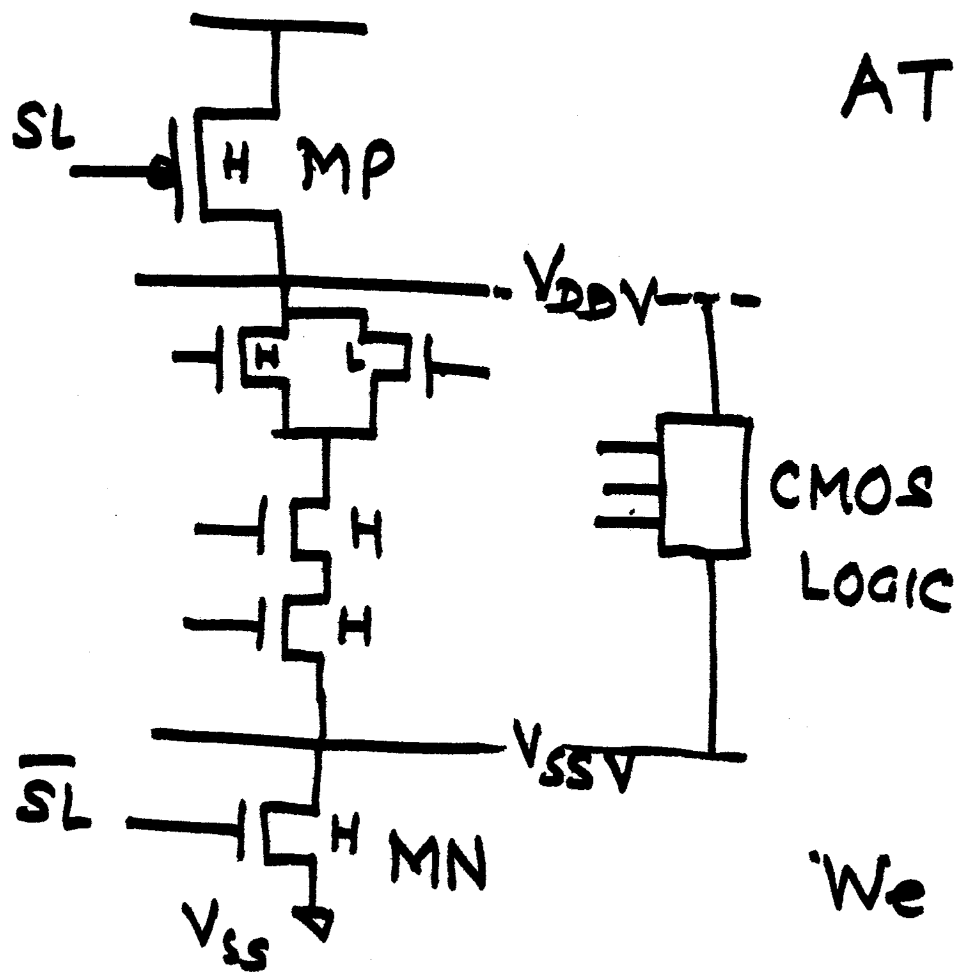
IN 'OFF' MODE SL = 1

MP AND MN ARE OFF WITH LOWER LEAKAGE WITH ADDITIONAL SERIES HIGH V_{TH} TRANSistors

DISADVANTAGES

1. LARGE AREA
2. SLOWER PERFORMANCE

MULTI THRESHOLD-VOLTAGE CMOS (MTCMOS)



AT SL=0 (ACTIVE MODE)

MP — ON

MN — ON

SLEEP TRANSISTORS ARE LARGE SIZE HIGH V_{TH} ONES

We CREATE V_{DDV} & V_{SSV}

MULTIPLE BODY BIAS

SUBSTRATE BIAS CHANGES V_{TH}

$$V_{TH}(V_{SB}) = V_{T0} + \gamma \left[(V_{SB} + 2\phi_F)^{1/2} - (2\phi_F)^{1/2} \right]$$

& $\gamma = \dfrac{[2 K_S \epsilon_0 q N_B]^{1/2}}{C_{ox}}$ = BODY BIAS Coeff.

APPLYING APPROPRIATE BODY BIAS TO VARIOUS TRANSISTORS, MULTIPLE V_{TH} TRANSISTORS ARE CREATED

2(b) GATE-OXIDE CHANGE LEADS TO CHANGE IN C_{ox}.

$\therefore V_{TH} \propto t_{ox}$

ASSIGN LOWER V_{TH} to TRANSISTORS IN CRITICAL PATH

OTHER TRANSISTORS HAVE HIGHER V_{TH} LEADING TO LOWER SUB-THRESHOLD CURRENTS.

2. MULTIPLE V_{TH} TECHNIQUE

(a) CHANNEL DOPING VARIES FOR DIFFERENT V_{TH} TRANSISTORS

$$V_{TH} = \phi_{MS} \pm 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B}{C_{ox}}$$

→ ϕ_{MS} = METAL-SEMICONDUCTOR WORKFUNCTION DIFFERENCE

→ $\phi_F = \frac{kT}{q} \ln \frac{N_B}{n_i}$, N_B - SUBSTRATE DOPING

→ Q_{ox} is FIXED POSITIVE CHARGE DENSITY

→ $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$, t_{ox} - Oxide Thickness
ϵ_{ox} - OXIDE PERMITIVITTY

→ $Q_B = \pm q N_B X_{DMAX}$, X_{DMAX} - DEPLETION WIDTH

$\therefore V_{TH} \propto \sqrt{N_B}$

$$X_{DM} = \sqrt{\frac{2 K_s \epsilon_0}{q N_B} (2\phi_F)}$$

(iii) $V_{DS_2} = V_{D2} - V_{S2} = V_{D2} - V_M$

SINCE V_M IS POSITIVE, V_{DS_2} IS SMALLER. HENCE $\underline{V_{TH2}}$ INCREASES DUE TO LOWERED DIBL VALUE.

IN ALL THREE CASES ONE OBSERVES REDUCTION IN SUB-THRESHOLD CURRENT $\Rightarrow$ REDUCED LEAKAGE POWER

(i) $V_{GS_2} = V_{G2} - V_{S2} = V_{G2} - V_M$

$= 0 - V_M = -V_M$

Subthreshold current of M2 reduces

Hence NET LEAKAGE CURRENT REDUCES

(ii) $V_{BS_2} = V_{B2} - V_{S2} = -V_M$

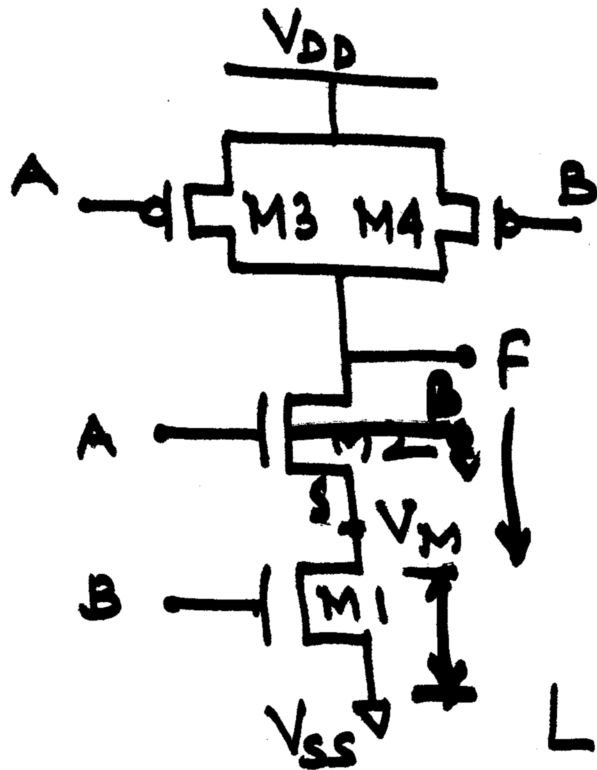
Extra Reverse Back-Bias

Enhances V_{TH} of M2. THIS LEADS TO REDUCED LEAKAGE CURRENT

LEAKAGE CONTROL

1. Stack Effect :

⇒ SELF REVERSE BIAS



2-INPUT NAND.

→ AS EXAMPLE

WHEN A = B = 0

M2 & M1 → ▬ OFF

M3 & M4 → ▬ ON

LEAKAGE CURRENT FLOWS FROM V_{DD} to V_{SS}

DUE TO STACKING OF NMOS TRANSISTORS M_1 & M_2, We Observe that at Node M between M1 & M2, has Voltage $+V_M$, due to Flow of Leakage Current. Positive V_M has THREE Effects Leading to Lowering of Leakage Current.

1. "LV/LP ICs & Systems"

E. Sanchez-Sinencio
ANDREAS . .

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2 LV/LP VLSI SUBSYSTEMS

K. Yeo & K. Roy

3. Digital IC - Design Perspective

J.M. Rabaey, A.Chandrakasan &
B. Nicolic

4. CMOS VLSI - -

Eshraghian & Waste.